of a semiconductor die, comprising:

applying a first layer of material to said surface of said semiconductor die;

applying a second layer of material as a mask to a portion of a surface of said first layer of material;

applying an encapsulant material to a remaining Portion of said surface of said semiconductor die;

curing said encapsulant material; and

peeling said first layer of material from said surface of said semiconductor die to remove said misplaced encapsulant material.

29. The method of claim 28, wherein said first layer of material and said second layer of material include a silicon gel material.

30. The method of claim 28, wherein said first layer of material and said second layer of material include an elastomeric material.

31. The method of claim 28, wherein said second layer of material includes a material selected from the group of natural rubber, synthetic rubber, and room temperature cured silicon rubber.

US006117797A

United States Patent [19]

Hembree

[11] Patent Number: 6,117,797

[45] Date of Patent: Sep. 12, 2000

[54] ATTACHMENT METHOD FOR HEAT SINKS AND DEVICES INVOLVING REMOVAL OF MISPLACED ENCAPSULANT

[75] Inventor: David R. Hembree, Boise, Id.

[73] Assignee: Micron Technology, Inc., Boise, Id.

[21] Appl. No.: 09/146,949

[22] Filed: Sep. 3, 1998

[51] Int. Cl.⁷ H01L 21/48

[52] U.S. Cl. 438/759; 438/122; 438/127

[58] Field of Search 438/122, 127, 438/759, 118

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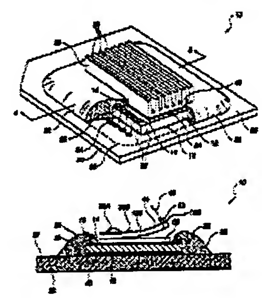
Assistant Examiner—Evan Pert

Attorney, Agent, or Firm—Trask Britt

[57] ABSTRACT

A process for forming a thermally enhanced Chip On Board semiconductor device with a heat sink is described. In one aspect, a thermally conducting interface material of filled gel elastomer material or a silicone elastomeric material or other elastomeric material is applied to the die surface to which the heat sink is to be bonded. A protective elastomeric layer is then applied to the interface material (or bare die). During subsequent glob top application and curing steps, it is conventionally difficult to remove unwanted glob top material, that which may have been unintentionally misapplied to the die surface. In the practice of this invention, the misplaced encapsulant (glob top) material adheres to the upper surface of the protective layer. The protective layer of material is then removed by peeling to also remove the misplaced glob top material prior to adhesive bonding of the heat sink to the die.

90 Claims, 6 Drawing Sheets



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film together via said adhesive layer, of coating at least a joint region between said semiconductor chip and said carrier film at a lateral side of a bonded unit of said semiconductor chip and said carrier film with a fluororesin coating material.

19. A method as claimed in claim 12, further including the step, after the step of bonding said semiconductor chip and said carrier film together via said adhesive layer, of coating at least a joint region between said semiconductor chip and said carrier film at a lateral side of a bonded unit of said semiconductor chip and said carrier film with a fluororesin coating material.

US005897337A

United States Patent [19]

Kata et al.

[11] Patent Number: 5,897,337

[45] Date of Patent: Apr. 27, 1999

[54] PROCESS FOR ADHESIVELY BONDING A SEMICONDUCTOR CHIP TO A CARRIER FILM

[75] Inventors: Keiichiro Kata; Shuichi Matsuda, both of Tokyo, Japan

[73] Assignee: NEC Corporation, Tokyo, Japan

[21] Appl. No.: [illegible]

[22] Filed: Sep. 26, 1995

[30] Foreign Application Priority Data

Sep. 30, 1994 [JP] Japan .... 6-[illegible]

[51] Int. Cl.[6] H01L 21/283; H01L 21/58; H01L 21/60

[52] U.S. Cl. 438/114; 438/115; 438/118; 438/462; 438/613; 438/667; 438/686

[58] Field of Search .... 438/114, 113, 438/116, 460, 613, 656, 667, 565, 906, 940, 975, FOR 343, FOR 364, FOR 363, FOR 365, FOR 372, FOR 384, FOR 403

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Attorney, Agent, or Firm—Whitham, Curtis & Whitham

[57] ABSTRACT

In a method of manufacturing a semiconductor device comprising a semiconductor chip and a carrier film which includes an insulating film and wiring patterns formed on one of main surfaces of the insulating film, an adhesive layer is formed on a surface of a semiconductor wafer having a number of integrated circuits. Each of the integrated circuits has electrode pads for external connection on the foregoing surface of the semiconductor wafer. Subsequently, openings are formed at regions of the adhesive layer corresponding to the electrode pads, and then, the semiconductor wafer is cut per integrated circuit so as to obtain the semiconductor chips. Thereafter, the electrode pads of the semiconductor chip and the wiring patterns of the carrier film are connected to each other through the corresponding openings of the adhesive layer, respectively. Then, the semiconductor chip and the carrier film are bonded together via the adhesive layer interposed therebetween. It may be arranged that the adhesive layer is formed on the carrier film rather than on the semiconductor chip.

23 Claims, 14 Drawing Sheets